ABSTRACT

An error correction scheme for transmission of electronic data using an in-line error correction where there are no explicit wires for error correction code (ECC) bits. A method for in-line error detection and correction is described which uses 0 to k wires, and symbols 0 to n, where information bits and symbols are sent along wires 0 to k. Before sending an information block along wires 0 to k, check bits are calculated from the information bits, wherein the check bits are made up of horizontal parity, extended parity and overall parity of the information. The check bits are sent along wires 0 to k, using the same wires as for the information bits.